PATENT CLAIMS:

1.-8. (cancelled)

9. (new) A method for synchronizing external events supplied to a CPU in a redundant configuration, comprising:

storing the external events for processing by an execution unit of the CPU;

retrieving the external events for processing by the execution unit of the CPU in a separate operating mode of the CPU;

storing a number of instructions executed by the execution unit since the CPU last leaves the separate operating mode in an instruction counter;

entering the separate operating mode after the number of instructions executed reaches a predefined maximum instruction counter;

switching to an individual command execution mode of the CPU if the number of instructions executed is greater than or equal to the predefined maximum instruction counter and a maximum deviation of instructions; and

remaining in the individual command execution mode until the number of instructions executed reaches the predefined maximum instruction counter, whereupon the CPU switches to the separate operating mode and the number of instructions executed is reinitialized.

10. (new) The method according to Claim 9, wherein the maximum deviation of instructions is greater than or equal to a number of instructions executed in parallel.

11. (new) The method according to Claim 9, wherein the external events are supplied to a plurality of CPUs.

12. (new) The method according to Claim 11, wherein each CPU receives an identical sequence of the instructions.

13. (new) The method according to Claim 11, wherein each CPU that is in the separate operating mode retrieves an identical set of the external events.

14. (new) The method according to Claim 11, wherein a CPU that is at the end of the separate operating mode remains in the separate operating mode until all redundant CPUs not at the end of the separate operating mode reach the end of the separate operating mode.

15. (new) The method according to Claim 9, wherein the number of instructions executed is monitored by a monitoring software CPU, the number of executed instructions prompted by the monitoring software CPU is identified separately and subtracted from the instruction counter.

16. (new) A CPU adapted to operate in a redundant configuration, comprising:

an execution unit;

a counter element that counts a number of instructions executed by the execution unit since the CPU last leaves a separate operating mode of the CPU, the counter element being reinitialized when the CPU leaves the separate operating mode;

a register element containing a value, the value being a maximum instruction count offset by a maximum deviation of instructions when the CPU is in a standard operation mode, and the value being the maximum instruction count when the CPU is in an individual command execution mode;

a comparator element that compares the counter element with the register element; and

a control element that switches the execution unit to the individual command execution mode when the comparator element determines that the counter element matches the register element,

wherein external events are stored for processing by the CPU and the external events are retrieved for processing by the CPU in the separate operating mode.

17. (new) The CPU according to Claim 16, wherein the maximum deviation of instructions is greater than or equal to a number of instructions executed in parallel.

18. (new) The CPU according to Claim 17, wherein the CPU executes a plurality of instructions in parallel.

19. (new) A computer system adapted to operate in a redundant configuration, comprising:

a plurality of CPUs, each CPU having an execution unit;

a counter element that counts a number of instructions executed by the execution unit since the CPU last leaves a separate operating mode of the CPU, the counter element being reinitialized when the CPU leaves the separate operating mode;

a register element containing a value, the value being a maximum instruction count offset by a maximum deviation of instructions when the CPU is in a standard operation mode, and the value being the maximum instruction count when the CPU is in an individual command execution mode;

a comparator element that compares the counter element with the register element; and

a control element that switches the execution unit to the individual command execution mode when the comparator element determines that the counter element matches the register element,

wherein external events are stored for processing by the CPU and the external events are retrieved for processing by the CPU in the separate operating mode.

20. (new) The system according to Claim 19, further comprising a connection between the plurality of CPUs executing an identical instruction sequence, whereby the connection is provided to transmit synchronization.

21. (new) The computer system according to Claim 19, wherein the maximum deviation of instructions is greater than or equal to a number of instructions executed in parallel.

22. (new) The computer system according to Claim 21, wherein the CPU executes a plurality of instructions in parallel.